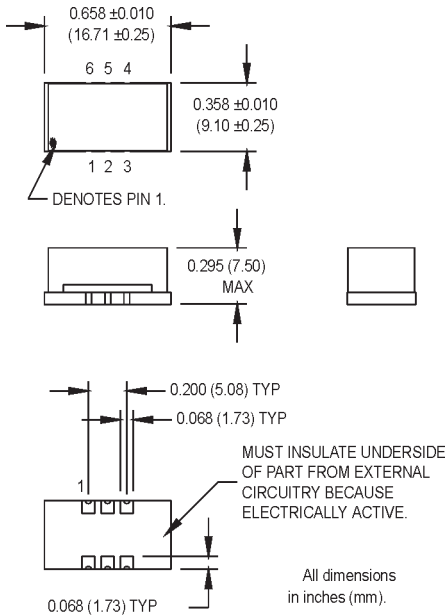


M5001 & M5002 Series

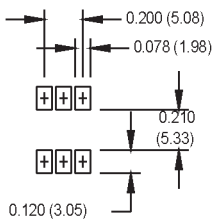
9x16 mm FR-4, 5.0 or 3.3 Volt, CMOS/TTL/PECL/LVDS, HPXO



- Excellent stability inclusive of all variations and 20 year life
- Ideal for SONET, PCS base stations and reference clock applications



SUGGESTED SOLDER PAD LAYOUT



Ordering Information

	M5001/M5002	2	8	R	C	K	00.0000 MHz
Product Series							
M5001 = 3.3 V							
M5002 = 5.0 V*							
Temperature Range							
1: 0°C to +70°C	2: -40°C to +85°C						
6: -20°C to +70°C	7: 0°C to +85°C						
Stability							
6: ±25 ppm	8: ±20 ppm						
D: ±15 ppm	E: ±10 ppm						
Output Type							
R: Complementary tri-state (LVPECL/LVDS)							
T: Tri-state (LVCMOS)							
Symmetry/Logic Compatibility							
D: 45/55% LVCMOS/TTL	L: 45/55% LVDS						
P: 45/55% LVPECL							
Package/Lead Configurations							
K: FR-4, 6 Pad							
Frequency (customer specified)							

* Contact the factory for 5.0 V availability.

Pad Connections

PIN	FUNCTION
1	N/C
2	Tri-state
3	Ground
4	Output 1
5	Output 2
6	+Vcc/Vdd

M-tron reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of such product.

M-tron Industries, Inc., PO Box 630, Yankton, SD 57078-0630, USA Phone: 605-665-9321 or 1-800-762-8800 Fax: 605-665-1709 Website: www.mtron.com
 M-tron Industries Limited, 1104 Shanghai Industrial Investment Building, 48-62 Hennessy Road, Wanchai, Hong Kong, China Phone: 852-2866-8023 Fax: 852-2529-1822

M5001 & M5002 Series

9x16 mm FR-4, 5.0 or 3.3 Volt, CMOS/TTL/PECL/LVDS, HPXO



PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
Frequency Range	F	1		160	MHz	LVCMOS
		1		800	MHz	LVPECL/LVDS
Frequency Stability ¹	$\Delta F/F$	(See Ordering Information)				
Operating Temperature	TA	(See Ordering Information)				
Input Voltage	Vcc/Vdd	3.0	3.3	3.6	VDC	LVCMOS/LVPECL/LVDS
Input Current ²	Icc/Idd	5		50	mA	LVCMOS
		5		75	mA	LVDS
		50		120	mA	LVPECL
Symmetry (Duty Cycle)		(See Ordering Information)				
Load		2 TTL or 15 pF Max.				LVCMOS/TTL
		50 Ohms to Vcc -2 VDC				LVPECL
		50 Ohm Differential Load				LVDS
Rise/Fall Time	Tr/Tf	2		10	ns	LVCMOS
		0.25		3	ns	LVPECL/LVDS
Logic "1" Level	Voh	2.5			VDC	LVCMOS
		2.2		2.4	VDC	LVPECL
		1.375			VDC	LVDS
Logic "0" Level	Vol			0.5	VDC	LVCMOS
		1.4		1.7	VDC	LVPECL
				1.125	VDC	LVDS
Phase Jitter	ϕJ			4	ps RMS	Integrated 12 kHz - 20 MHz Or 50 kHz to 80 Mhz
Phase Noise		-105 dBc/Hz at 10 kHz typical at 622.080 MHz				LVPECL
Aging				6	ppm	20 years
Tri-State Function		Logic Level "1" for enabled output(s) Logic Level "0" for disabled output(s)				
Environmental	Mechanical Shock	Per MIL-STD-202, Method 213, Condition E				
	Thermal Shock	Per MIL-STD-883, Method 1011, Condition A				
	Vibration	Per MIL-STD-883, Method 2007, Condition A				
	Reflow Solder Conditions	See "Figure 2" on page 147				

1. Stability includes initial tolerance, deviation over temperature, supply and load variation, and aging for 20 years @ 25°C.
2. Actual value of this parameter is frequency dependent.

HPXO

M-tron reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of such product.

M-tron Industries, Inc., PO Box 630, Yankton, SD 57078-0630, USA Phone: 605-665-9321 or 1-800-762-8800 Fax: 605-665-1709 Website: www.mtron.com
M-tron Industries Limited, 1104 Shanghai Industrial Investment Building, 48-62 Hennessy Road, Wanchai, Hong Kong, China Phone: 852-2866-8023 Fax: 852-2529-1822